ABSTRACT

Circuits, architectures, a system and methods for clock data recovery. The circuit generally includes (a) a clock phase adjustment circuit, receiving clock phase information and providing a clock phase adjustment signal, (b) a clock frequency adjustment circuit, receiving clock frequency information and providing a clock frequency adjustment signal, and (c) an adder circuit, receiving the clock phase adjustment signal and the clock frequency adjustment signal, and providing a clock recovery adjustment signal. The architectures and/or systems generally comprise those that include a clock data recovery circuit embodying one or more of the inventive concepts disclosed herein. The method generally comprises the steps of (1) sampling the data stream at predetermined times, (2) generating clock frequency information and clock phase information from sampled data, and (3) altering a frequency and/or a phase of the clock signal in response to the clock frequency information and the clock phase information. The present invention prevents or reduces the likelihood of a potential nonconvergence/clock runaway problem, advantageously with minimal or no changes to existing designs and logic. The present invention further advantageously improves system stability, reliability and performance with a minimum of additional circuitry.